CLAIMS

1.   A method of measuring parameters of an electronic system by reference to a series of data samples comprising the steps of:

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(a)   recovering a clock signal from an input signal received from the electronic system;

(b)   sampling and digitising said recovered clock signal to produce a series of digital clock samples;

(c)   processing said digital clock samples digitally with reference to a local

10   digital reference signal to produce digital baseband frequency in-phase (I) and quadrature (Q) components;

(d)   processing said digital I and Q components to extract digital phase information of said clock signal; and

(f)   processing said digital phase information to determine a parameter of the

15   electronic system.

2.   A method as claimed in claim 1 wherein step (c) is implemented using a digital signal down-converter IC of a type suitable for digital radio receiver implementations.

20   3.   A method as claimed in claim 1 wherein the steps (d) and (e) are implemented in a single programmable digital signal processor chip.

4.   A method as claimed in claim 1 wherein the network further comprises the step (a1) frequency-dividing said recovered clock signal prior to said sampling step.

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5.   A method as claimed in claim 1 wherein the frequency dividing step is performed so as to fix the frequency of the digital clock signal for sampling while measuring recovered clock signals of different frequencies.

30   6.   A method as claimed in claim 1 wherein the processing of said digital clock samples to produce baseband frequency in-phase (I) and quadrature (Q) components

comprises splitting said digital clock samples into at least two components and mixing them with respective reference signals derived from a said local digital reference signal.

7.   A method as claimed in claim 1 wherein the processing of said baseband frequency I and Q components to extract phase information further comprises the step of filtering and decimating said I and Q components.

8.   A method as claimed in claim 1 wherein the step of extracting phase information comprises applying an inverse tangent function to said filtered and decimated I and Q components by digital signal processing.

9.   A method as claimed in claim 1 wherein the phase of said local digital reference signal is controlled in response to the extracted phase information as part of a phase-locked loop (PLL).

10.   A method as claimed in claim 9 wherein the extracted digital phase information is processed into clock jitter data at step (e) by digitally filtering the phase information outside the phase-locked loop.

11.   A method as claimed in claim 9 wherein said filtering comprises high-pass digital filtering of the phase information.

12.   A method as claimed in claim 11 wherein the filtering further comprises a low-pass digital filter stage additional to that in the phase-locked loop.

13.   A method as claimed in claim 1 wherein said local digital reference signal is an externally sourced timing signal, independent of the received signal.

14.   A method as claimed in claim 13 wherein the extracted digital phase information is processed into clock time interval error (TIE) data by filtering this phase information.

15.   A method as claimed in claim 14 wherein the filtering comprises low-pass digital filtering of the phase information.

16.   A method as claimed in claim 14 wherein the resultant time interval error data is
5   further processed to derive wander data.

17.   A method as claimed in claim 1 implemented in a form of hardware switchable between phase-locked and independent reference signals according to the measurement desired.

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18.   A method as claimed in claim 1 wherein the method is used as pre-processing for a composite measurement comprising at least one of MTIE, MRTIE, TDEV, RMS and Pk-Pk, as defined by any ITU standard.

15   19.   A method as claimed in claim 18 wherein said pre-processing and the derivation of said composite measurement are performed within a single digital signal processor.

20.   An apparatus for measuring parameters of an electronic system by reference to a series of data samples, comprising:
20   clock recovery means for recovering a clock signal from an input signal received from the electronic system;
            a sampler for sampling and digitising said recovered clock signal to produce a series of digital clock samples; and
            a processor for processing said digital clock samples digitally with reference to
25   a local digital reference signal to produce digital baseband frequency in-phase (I) and quadrature (Q) components, processing said digital I and Q components to extract digital phase information of said clock signal, and processing said digital phase information to determine a parameter of the electronic system.